B1 cont.

substrate. Hence, when an unannealed glass substrate is used in place of the annealed glass substrate, the temperature condition of about 600°C may cause a shrinkage of the glass substrate, and this may cause a warpage or strain of the glass substrate to bring about difficulties such as break of the glass substrate itself and peel of the layer, at worst.

On Page 3, please replace the last paragraph, beginning at line 22 and bridging to page 4, line 8, with the following:

B2

Usually, alkali-free glass substrates used as substrates of thin-film transistors have a strain point of about 600°C, and compaction (heat shrinkage) of glass becomes great abruptly as a result of heat history at upper temperatures than at a temperature a little lower than the strain point. For example, an unannealed glass substrate CORNING 7059F (Trade name: available from Corning Glass works; strain point 593°C) shows a compaction of about 800 ppm as a result of heat history at 600°C, for 1 hour and at a cooling rate of 1°C/minute. Also, in the case of CORNING 1735F (strain point: 665°C), having a higher strain point, it shows a compaction of 173 ppm upon application of the same heat history as the above. Then, it has been made possible to lower compaction due to the like heat history to about 10 ppm by carrying out annealing previously at 660°C/1 hr.

On Page 4, please replace the last paragraph, beginning at line 17, with the following:

B3

That is, as a gate-insulating layer formed on a polycrystalline silicon layer, as stated previously an SiO_2 layer is formed in a layer thickness of about 100 nm by plasma-assisted CVD (chemical vapor deposition) using TEOS (tetraethoxysilane)

as a material gas (herein "TEOS layer"). At the interface between the polycrystalline silicon layer and the insulating layer formed of TEOS, however, the interfacial density of the TEOS layer becomes so high that the threshold voltage required of a TFT tends to vary and also the breakdown strength of the gate-insulating layer thereof may severely deteriorate with time. Thus, there is a great problem on the reliability of TFT.

B3 cont

On Page 5, please replace the third paragraph, beginning at line 15, with the following:

B4

To achieve the above object, in the present invention, i) a polysilicon crystal layer for forming a channel region, a source region and a drain region and ii) a first insulating layer and a second insulating layer are formed at the upper part of an unannealed glass substrate. Also, a gate region is formed at a position corresponding to the channel region and on the second insulating layer. And a gate electrode, a source electrode and a drain electrode are also formed to make electrical interconnection with the gate region, the source region and the drain region, respectively.

On Page 5, please replace the last paragraph, beginning at line 24, and bridging to page 6, line 1, with the following:

B5

Here, it is preferable that the first insulating layer is a silicon oxide layer formed by oxidizing the surface of the channel region at a temperature of 500°C or below, and is so formed as to cover the surface of at least the channel region and to have a layer thickness of 4 nm or larger.

On Page 6, please replace the first full paragraph, beginning at line 2, with the following:

B6

In the present invention, it is preferable that the first insulating layer, e.g., a silicon oxide layer, is formed by oxidizing the surface of a polycrystalline silicon layer in an atmosphere containing at least ozone, for example, an atmosphere containing ozone and H_2O or an atmosphere containing ozone and N_2O. Also, in the present invention, in the step of forming the first insulating layer, it is preferable that a first silicon oxide layer is formed at the surface of the polycrystalline silicon layer by the use of an oxygen-donating solution, and thereafter a second silicon oxide layer is formed between the first silicon oxide layer and the polycrystalline silicon layer in an atmosphere containing ozone.

On Page 6, please replace the last paragraph, beginning at line 22, and bridging to page 7, line 4, with the following:

B7

In other words, the thin-film transistor manufactured by the above method has a good interface between the surface of the channel region comprised of polycrystalline silicon and the gate insulating layer formed thereon, and hence the thin-film transistor characteristics concerned closely with the interfacial state density thereat, as exemplified by threshold voltage, can be made to vary less, so that superior TFT characteristics can be exhibited. In addition, since the unannealed glass substrate can be used as the substrate, the TFT can be formed in a large area and at a low cost, compared with quartz glass substrates or the like.

On Page 7, please replace the second paragraph, beginning at line 5, with the following:

B8 In the above means for solving the problem, the insulating layer has a double-layer structure, which, however, need not necessarily be limited thereto.

On Page 7, please replace the fifth paragraph, beginning at line 15, with the following:

B9 Figs. 2A to 2D show flow diagrams for describing various stages of a process of manufacturing the thin-film transistor according to a first embodiment;

On Page 7, please replace the last paragraph, beginning at line 24, with the following:

B10 Fig. 7 is a schematic view for describing changes in surface temperature of a silicon substrate in an embodiment.

On Page 8, please replace the fourth paragraph, beginning at line 18, with the following:

B11 A method of producing the above structure shown in Fig. 1 is described below with reference to the flow diagrams shown in Figs. 2A to 2D.

On Page 10, please replace the last paragraph, beginning at line 21, and bridging to page 11, line 2, with the following:

B12 Incidentally, although it is unnecessary to specifically set an upper limit of the thermal-oxide layer thickness, the thickness need not be made too large when the gate insulating layer is formed in the thermal oxide/TEOS double-layer structure. More specifically, taking account of the productivity of thin-film transistors, it is suitable for the layer thickness to be, e.g., about 20 nm in maximum, considering that

B12 cont. the process of thermal oxidation is a process in which the oxide layer is formed at a low rate.

<u>On Page 11,</u> please replace the first full paragraph, beginning at line 3, with the following:

B13 In the above first embodiment, described is a case in which the gate-insulating layer 6 has a double-layer structure. It may also have a single-layer structure as shown in Fig. 4. In the latter case, the step of forming the second insulating layer 6b may only be omitted in the steps described above.

<u>On Page 13,</u> please replace the third full paragraph, beginning at line 9, with the following:

B14 As a method of forming the oxide layer of about 1 nm in layer thickness, for example, a sample on which the polycrystalline silicon layer 4 has been formed may be immersed in ozone water prepared by bubbling ozone gas into pure water. Also, in place of the ozone water, the sample may be immersed in an aqueous ammonia/hydrogen peroxide solution.

<u>On Page 15,</u> please replace the third paragraph, beginning at line 12, with the following:

B15 In order to accelerate the oxidation reaction at the substrate surface, it is necessary to prevent the ozone itself from decomposing and the temperature of the substrate surface from lowering, in the course before the ozone reaches the surface of the substrate. In other words, it is preferable to keep the temperature at 200°C or below, and more preferably 150°C or below, which is a temperature of such a degree

B15 cont.

that the ozone gas fed to the surface of the substrate does not decompose, and also to keep only the substrate surface at a high temperature.

On Page 15, please replace the last paragraph, beginning at line 25, and bridging to page 26, line 6, with the following:

B16

In general, where a gas is fed to the surface of a substrate in the state the substrate is held on a stage the temperature of which is controlled by means of a general-purpose heater, the temperature of the substrate surface changes as shown in Fig. 5. More specifically, in Fig. 5, the lapse of time is plotted as abscissa, and the input to a heater, the internal temperature of a stage to which the heater is attached and the surface temperature of the substrate are plotted as ordinate, showing changes of the surface temperature of the substrate.

On Page 18, please replace the last paragraph, beginning at line 26, and bridging to page 19, with the following:

B17

While we have shown and described several embodiments in accordance with our invention, it should be understood that disclosed embodiments are susceptible of changes and modifications without departing from the scope of the invention. Therefore, we do not intend to be bound by the details shown and described herein but intend to cover all such changes and modifications that fall within the ambit of the appended claims.

IN THE CLAIMS:

Please **cancel** claims 3 – 8, 10 and 12, without prejudice or disclaimer of the subject matter therein.